M2U1G64DS8HB1G / M2U51264DS88B1G / M2U25664DSH4B1G
M2Y1G64DS8HB1G / M2Y51264DS88B1G / M2Y25664DSH4B1G (Green)
1GB, 512MB and 256MB
PC3200 and PC2700
Unbuffered DDR DIMM

184 pin Unbuffered DDR DIMM

Based on DDR400/333 512M bit Die B device

Features

- 184 Dual In-Line Memory Module (DIMM)
- Unbuffered DDR DIMM based on 110nm 512M bit die B device
- Performance:

Speed Sort	PC2700 6K	PC3200 5T	Unit
DIMM $\overline{CAS}$ Latency	2.5	3	
f_{CK} Clock Frequency	166	200	MHz
t_{CK} Clock Cycle	6	5	ns
f_{DQ} DQ Burst Frequency	333	400	MHz

- Intended for 200 and 166 MHz applications
- Inputs and outputs are SSTL-2 compatible
- $V_{DD} = V_{DDQ} = 2.5V \pm 0.2V$ (6K); $V_{DD} = V_{DDQ} = 2.6V \pm 0.1V$ (5T)
- SDRAMs have 4 internal banks for concurrent operation
- Differential clock inputs
- Data is read or written on both clock edges
- DRAM DLL aligns DQ and DQS transitions with clock transitions
- Address and control signals are fully synchronous to positive clock edge
- Programmable Operation:
  - DIMM $\overline{CAS}$ Latency: 2, 2.5 (6K); 2.5, 3 (5T)
  - Burst Type: Sequential or Interleave
  - Burst Length: 2, 4, 8
  - Operation: Burst Read and Write
- Auto Refresh (CBR) and Self Refresh Modes
- Automatic and controlled precharge commands
- 7.8 µs Max. Average Periodic Refresh Interval
- Serial Presence Detect EEPROM
- Gold contacts on module PCB

Description

M2U1G64DS8HB1G and M2Y1G64DS8HB1G are unbuffered 200-Pin Double Data Rate (DDR) Synchronous DRAM Unbuffered Dual In-Line Memory Module (UDIMM) and are organized as two ranks of 128Mbx64 high-speed memory array using sixteen 64Mx8 DDR SDRAMs TSOP packages. M2U51264DS88B1G and M2Y51264DS88B1G are unbuffered 200-Pin DDR Synchronous DRAM UDIMM and are organized as a single rank of 64Mbx64 high-speed memory array using eight 64Mx8 DDR SDRAMs TSOP packages. M2U25664DSH4B1G and M2Y25664DSH4B1G are unbuffered 200-Pin DDR Synchronous DRAM UDIMM and are organized as a single rank of 32Mbx64 high-speed memory array using four 32Mx16 DDR SDRAMs TSOP packages.

Depending on the speed grade, these DIMMs are intended for use in applications operating up to 200 MHz clock speeds and achieves high-speed data transfer rates of up to 400 MHz. Prior to any access operation, the device $\overline{CAS}$ latency and burst /length/operation type must be programmed into the DIMM by address inputs and I/O inputs BA0 and BA1 using the mode register set cycle.

The DIMM uses a serial EEPROM and through the use of a standard IIC protocol the serial presence-detect implementation (SPD) can be accessed. The first 128 bytes of the SPD data are programmed with the module characteristics as defined by JEDEC.

Ordering Information

Non-Green Products

Part Number	Size	Speed			Power	Leads
M2U1G64DS8HB1G-5T	128Mx64	DDR400 Devices	PC3200 3-3-3	200MHz (5ns @ CL = 3)	2.6V	Gold
M2U51264DS88B1G-5T	64Mx64					
M2U25664DSH4B1G-5T	32Mx64					
M2U51264DS88B1G-6K	64Mx64	DDR333 Devices	PC2700 2.5-3-3	166MHz (6ns @ CL = 2.5)	2.5V	
M2U25664DSH4B1G-6K	32Mx64					

Green products

Part Number	Size	Speed			Power	Leads
M2Y1G64DS8HB1G-5T	128Mx64	DDR400 Devices	PC3200 3-3-3	200MHz (5ns @ CL = 3)	2.6V	Gold
M2Y51264DS88B1G-5T	64Mx64					
M2Y25664DSH4B1G-5T	32Mx64					
M2Y51264DS88B1G-6K	64Mx64	DDR333 Devices	PC2700 2.5-3-3	166MHz (6ns @ CL = 2.5)	2.5V	
M2Y25664DSH4B1G-6K	32Mx64					

Pin Description

CK0, CK1, CK2, $\overline{CK0}$, $\overline{CK1}$, $\overline{CK2}$	Differential Clock Inputs.	DQ0-DQ63	Data input/output
CKE0, CKE1	Clock Enable	DQS0-DQS7	Bidirectional data strobes
$\overline{RAS}$	Row Address Strobe	DM0-DM7	Input Data Mask
$\overline{CAS}$	Column Address Strobe	V_{DD}	Power
$\overline{WE}$	Write Enable	V_{DDQ}	Supply voltage for DQs
$\overline{S0}$, $\overline{S1}$	Chip Selects	V_{SS}	Ground
A0-A9, A11, A12	Address Inputs	NC	No Connect
A10/AP	Address Input/Auto-precharge	SCL	Serial Presence Detect Clock Input
BA0, BA1	SDRAM Bank Address Inputs	SDA	Serial Presence Detect Data input/output
V_{REF}	Ref. Voltage for SSTL_2 inputs	SA0-2	Serial Presence Detect Address Inputs
V_{DDID}	V_{DD} Identification flag.	V_{DDSPD}	Serial EEPROM positive power supply

Pinout

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V_{REF}	93	V_{SS}	32	A5	124	V_{SS}	62	V_{DDQ}	154	$\overline{RAS}$
2	DQ0	94	DQ4	33	DQ24	125	A6	63	$\overline{WE}$	155	DQ45
3	V_{SS}	95	DQ5	34	V_{SS}	126	DQ28	64	DQ41	156	V_{DDQ}
4	DQ1	96	V_{DDQ}	35	DQ25	127	DQ29	65	$\overline{CAS}$	157	$\overline{S0}$
5	DQS0	97	DM0	36	DQS3	128	V_{DDQ}	66	V_{SS}	158	$\overline{S1}$/NC
6	DQ2	98	DQ6	37	A4	129	DM3	67	DQS5	159	DM5
7	V_{DD}	99	DQ7	38	V_{DD}	130	A3	68	DQ42	160	V_{SS}
8	DQ3	100	V_{SS}	39	DQ26	131	DQ30	69	DQ43	161	DQ46
9	NC	101	NC	40	DQ27	132	V_{SS}	70	V_{DD}	162	DQ47
10	NC	102	NC	41	A2	133	DQ31	71	NC	163	NC
11	V_{SS}	103	NC	42	V_{SS}	134	NC	72	DQ48	164	V_{DDQ}
12	DQ8	104	V_{DDQ}	43	A1	135	NC	73	DQ49	165	DQ52
13	DQ9	105	DQ12	44	NC	136	V_{DDQ}	74	V_{SS}	166	DQ53
14	DQS1	106	DQ13	45	NC	137	CK0	75	$\overline{CK2}$	167	NC
15	V_{DDQ}	107	DM1	46	V_{DD}	138	$\overline{CK0}$	76	CK2	168	V_{DD}
16	CK1	108	V_{DD}	47	NC	139	V_{SS}	77	V_{DDQ}	169	DM6
17	$\overline{CK1}$	109	DQ14	48	A0	140	NC	78	DQS6	170	DQ54
18	V_{SS}	110	DQ15	49	NC	141	A10/AP	79	DQ50	171	DQ55
19	DQ10	111	CKE1/NC	50	V_{SS}	142	NC	80	DQ51	172	V_{DDQ}
20	DQ11	112	V_{DDQ}	51	NC	143	V_{DDQ}	81	V_{SS}	173	NC
21	CKE0	113	NC	52	BA1	144	NC	82	V_{DDID}	174	DQ60
22	V_{DDQ}	114	DQ20	KEY		KEY		83	DQ56	175	DQ61
23	DQ16	115	A12/NC	53	DQ32	145	V_{SS}	84	DQ57	176	V_{SS}
24	DQ17	116	V_{SS}	54	V_{DDQ}	146	DQ36	85	V_{DD}	177	DM7
25	DQS2	117	DQ21	55	DQ33	147	DQ37	86	DQS7	178	DQ62
26	V_{SS}	118	A11	56	DQS4	148	V_{DD}	87	DQ58	179	DQ63
27	A9	119	DM2	57	DQ34	149	DM4	88	DQ59	180	V_{DDQ}
28	DQ18	120	V_{DD}	58	V_{SS}	150	DQ38	89	V_{SS}	181	SA0
29	A7	121	DQ22	59	BA0	151	DQ39	90	NC	182	SA1
30	V_{DDQ}	122	A8	60	DQ35	152	V_{SS}	91	SDA	183	SA2
31	DQ19	123	DQ23	61	DQ40	153	DQ44	92	SCL	184	V_{DDSPD}

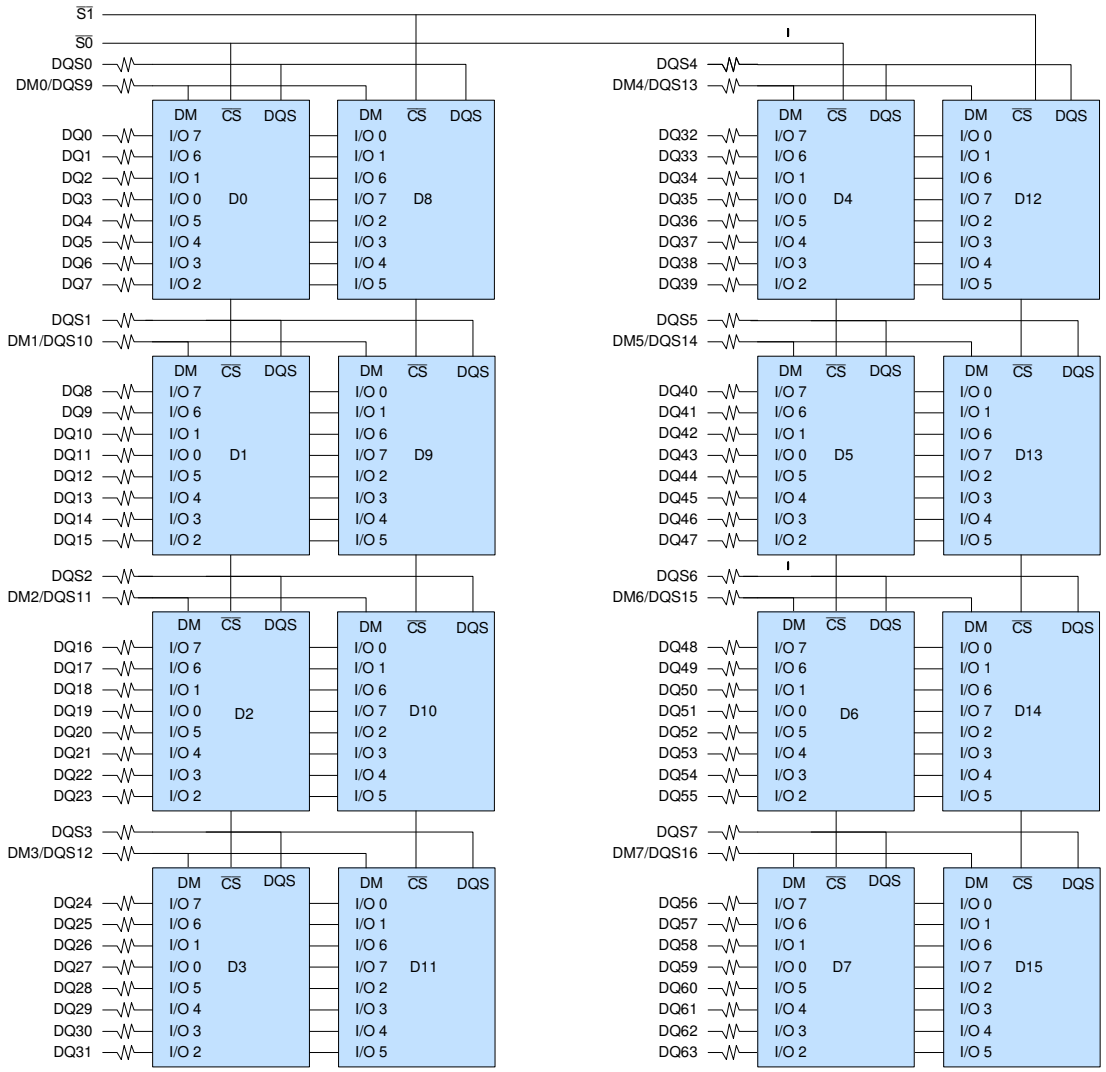
Note: All pin assignments are consistent for all 8-byte unbuffered versions.

Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0, CK1, CK2, $\overline{CK0}$, $\overline{CK1}$, $\overline{CK2}$	(SSTL)	Cross point	The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and falling edge of CK. A Delay Locked Loop (DLL) circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock.
CKE0, CKE1	(SSTL)	Active High	Activates the DDR SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode or the Self Refresh mode.
$\overline{S0}$, $\overline{S1}$	(SSTL)	Active Low	Enables the associated DDR SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. Physical Bank 0 is selected by S0; Bank 1 is selected by S1.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	(SSTL)	Active Low	When sampled at the positive rising edge of the clock, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ define the operation to be executed by the SDRAM.
V_{REF}	Supply		Reference voltage for SSTL-2 inputs
V_{DDQ}	Supply		Isolated power supply for the DDR SDRAM output buffers to provide improved noise immunity
BA0, BA1	(SSTL)	-	Selects which SDRAM bank is to be active.
A0 - A9 A10/AP A11, A12	(SSTL)	-	During a Bank Activate command cycle, A0-A12 defines the row address (RA0-RA12) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A9 defines the column address (CA0-CA9) when sampled at the rising clock edge. In addition to the column address, AP is used to invoke auto-precharge operation at the end of the Burst Read or Write cycle. If AP is high, auto-precharge is selected and BA0/BA1 defines the bank to be precharged. If AP is low, auto-precharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0/BA1 to control which bank(s) to precharge. If AP is high all 4 banks will be precharged regardless of the state of BA0/BA1. If AP is low, then BA0/BA1 are used to define which bank to pre-charge.
DQ0 - DQ63	(SSTL)	-	Data and Check Bit input/output pins operate in the same manner as on conventional DRAMs.
DQS0 - DQS7,	(SSTL)	Active High	Data strobes: Output with read data, input with write data. Edge aligned with read data, centered on write data. Used to capture write data.
DM0 – DM8	Input	Active High	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect. DM8 is associated with check bits CB0-CB7, and is not used on x64 modules.
V_{DD}, V_{SS}	Supply		Power and ground for the DDR SDRAM input buffers and core logic
SA0 – SA2		-	Address inputs. Connected to either V_{DD} or V_{SS} on the system board to configure the Serial Presence Detect EEPROM address.
SDA		-	This bi-directional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V DD to act as a pull-up.
SCL		-	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to V DD to act as a pull-up.
V_{DDSPD}	Supply		Serial EEPROM positive power supply.

Functional Block Diagram

2 Ranks, 16 devices, 64Mx8 DDR SDRAMs, 1GB

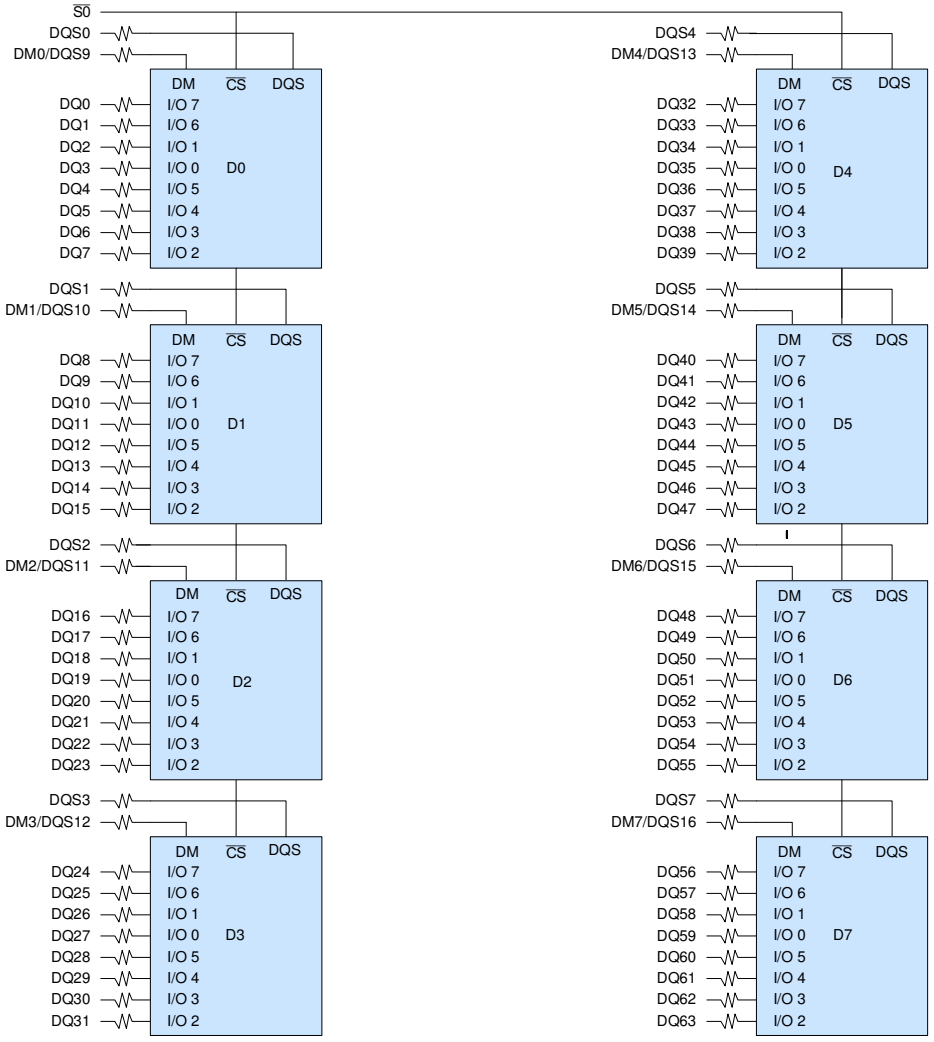


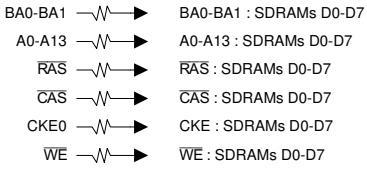
Notes :

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ, DQS, DM/DQS resistors: 22 Ohms.
4. V_{DDID} strap connections (for memory device V_{DD}, V_{DDQ}):
   STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$
   STRAP IN (V_{SS}): V_{DD} is not equal to V_{DDQ}.

Functional Block Diagram

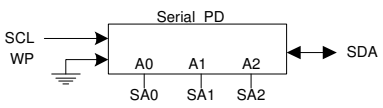
1 Rank, 8 devices, 64Mx8 DDR SDRAMs, 512MB

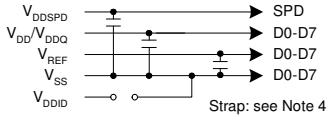




* Clock Wiring	
Clock Input	SDRAMs
*CK0/CK0	2 SDRAMs
*CK1/CK1	3 SDRAMs
*CK2/CK2	3 SDRAMs

* Wire per Clock Loading Table/ Wiring Diagrams



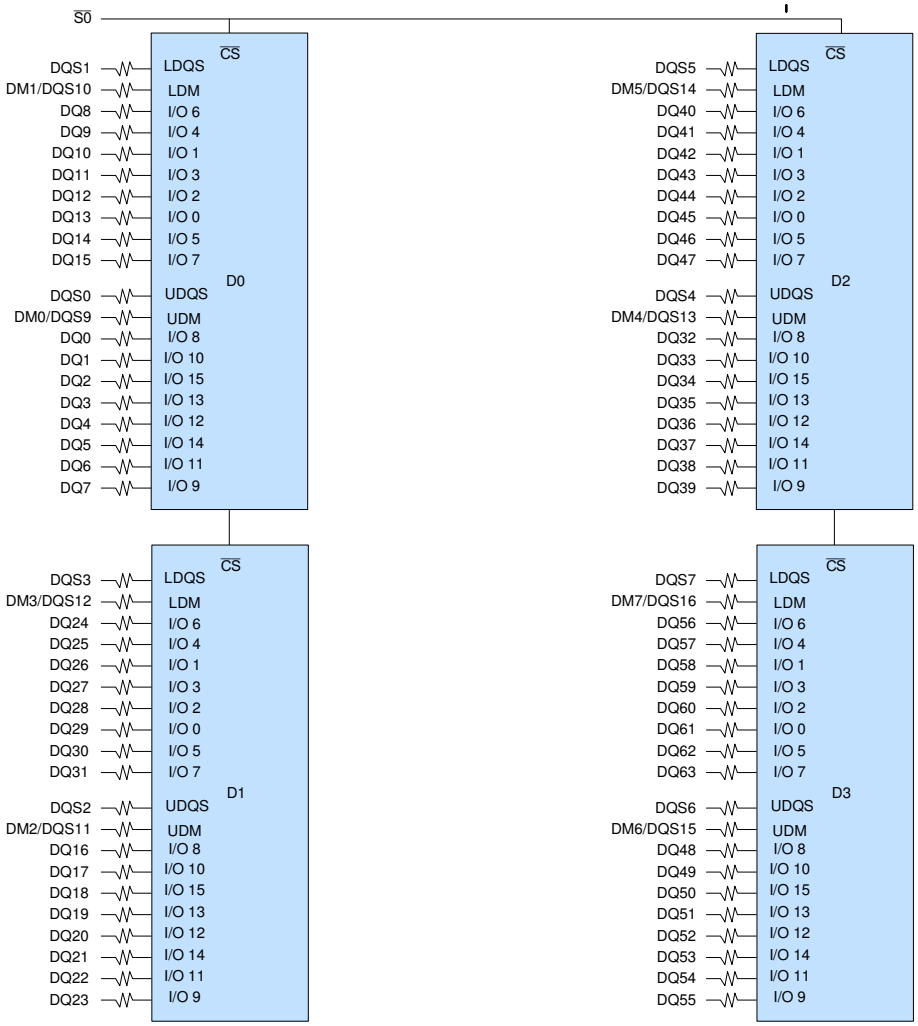


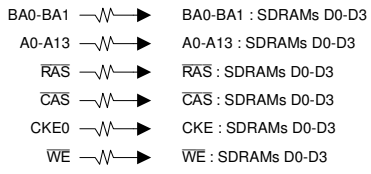
Notes :

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ, DQS, DM/DQS resistors: 22 Ohms.
4. V_{DDID} strap connections (for memory device V_{DD}, V_{DDQ}):
   STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$
   STRAP IN (V_{SS}): V_{DD} is not equal to V_{DDQ}.

Functional Block Diagram

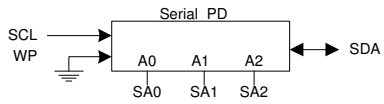
1 Rank, 4 devices, 32Mx16 DDR SDRAMs, 256MB

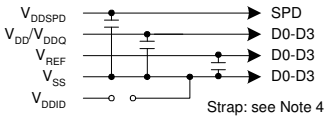




* Clock Wiring	
Clock Input	SDRAMs
*CK0/CK0	NC
*CK1/CK1	2 SDRAMs
*CK2/CK2	2 SDRAMs

* Wire per Clock Loading Table/ Wiring Diagrams





Notes :

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ, DQS, DM/DQS resistors: 22 Ohms.
4. V_{DDID} strap connections (for memory device V_{DD}, V_{DDQ}):
   STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$
   STRAP IN (V_{SS}): V_{DD} is not equal to V_{DDQ}.

Serial Presence Detect

SPD Values for 1GB

Byte	Description	SPD Entry Value		Serial PD Data Entry (Hexadecimal)	
		DDR400 -5T	DDR333 -6K	DDR400 -5T	DDR333 -6K
0	Number of Serial PD Bytes Written during Production	128		80	
1	Total Number of Bytes in Serial PD device	256		08	
2	Fundamental Memory Type	DDR SDRAM		07	
3	Number of Row Addresses on Assembly	13		0D	
4	Number of Column Addresses on Assembly	11		0B	
5	Number of DIMM Bank	2		02	
6.	Data Width of Assembly	X64		40	
7	Data Width of Assembly (cont')	X64		00	
8	Voltage Interface Level of this Assembly	SSTL 2.5V		04	
9	DDR SDRAM Device Cycle Time at CL=3	5ns	6ns	50	60
10	DDR SDRAM Device Access Time from Clock at CL=3	0.65ns	0.7ns	65	70
11	DIMM Configuration Type	Non-Parity		00	
12	Refresh Rate/Type	SR/1x(7.8us), Self Refresh Flag		82	
13	Primary DDR SDRAM Width	X8		08	
14	Error Checking DDR SDRAM Device Width	N/A		00	
15	DDR SDRAM Device Attr: Min Clk Delay, Random Col Access	1 Clock		01	
16	DDR SDRAM Device Attributes: Burst Length Supported	2,4,8		0E	
17	DDR SDRAM Device Attributes: Number of Device Banks	4		04	
18	DDR SDRAM Device Attributes: CAS Latencies Supported	2.5/3	2/25	18	0C
19	DDR SDRAM Device Attributes: CS Latency	0		01	
20	DDR SDRAM Device Attributes: WE Latency	1		02	
21	DDR SDRAM Device Attributes:	Differential Clock		20	
22	DDR SDRAM Device Attributes: General	+/-0.2V Voltage Tolerance		C0	
23	Minimum Clock Cycle at CL=2.5	6.0ns	7.5ns	60	75
24	Maximum Data Access Time (t_{AC}) from Clock at CL=2.5	0.7ns	0.75ns	70	75
25	Minimum Clock Cycle Time at CL=2	N/A		00	
26	Maximum Data Access Time (t_{AC}) from Clock at CL=2	N/A		00	
27	Minimum Row Precharge Time (t_{RP})	15ns	18ns	3C	48
28	Minimum Row Active to Row Active delay (t_{RRD})	10ns	12ns	28	30
29	Minimum RAS to CAS delay (t_{RCD})	15ns	18ns	3C	48
30	Minimum RAS Pulse Width (t_{RAS})	40ns	42ns	28	2A
31	Module Bank Density	512MB		80	
32	Address and Command Setup Time Before Clock	0.6ns	0.75ns	60	75
33	Address and Command Hold Time After Clock	0.6ns	0.75ns	60	75
34	Data Input Setup Time Before Clock	0.4ns	0.45ns	40	45
35	Data Input Hold Time After Clock	0.4ns	0.45ns	40	45
36-40	Reserved	Undefined		00	
41	Minimum Active/Auto-Refresh Time (tRC)	55ns	60ns	37	3C
42	SDRAM Device Minimum Auto-Refresh to Active/Auto Refresh Command Period (tRFC)	70ns	72ns	46	48
43	SDRAM Device Maximum Cycle Time (tCK max)	12		30	
44	SDRAM Device Maximum DQS-DQ Skew Time (tDQSQ)	0.4	0.45	28	2D
45	SDRAM Device Maximum Read Data Hold Skew Factor (tQHS)	0.5	0.55	50	55
46	Superset Information (may be used in future)	Undefined		00	
47	SDRAM device Attributes – DDR SDRAM DIMM Height	31.75mm		01	
48-61	Superset Information (may be used in future)	Undefined		00	
62	SPD Revision	1.0		10	
63	Checksum Data	Check sum		C8	58
64-71	Manufacturer's JEDED ID Code	0B Hex bank 3		7F7F7F0B00000000	
72-255	Reserved	Undefined		--	

SPD Values for 512MB

Byte	Description	SPD Entry Value		Serial PD Data Entry (Hexadecimal)	
		DDR400 -5T	DDR333 -6K	DDR400 -5T	DDR333 -6K
0	Number of Serial PD Bytes Written during Production	128		80	
1	Total Number of Bytes in Serial PD device	256		08	
2	Fundamental Memory Type	DDR SDRAM		07	
3	Number of Row Addresses on Assembly	13		0D	
4	Number of Column Addresses on Assembly	11		0B	
5	Number of DIMM Bank	1		01	
6.	Data Width of Assembly	X64		40	
7	Data Width of Assembly (cont')	X64		00	
8	Voltage Interface Level of this Assembly	SSTL 2.5V		04	
9	DDR SDRAM Device Cycle Time at CL=3	5ns	6ns	50	60
10	DDR SDRAM Device Access Time from Clock at CL=3	0.65ns	0.7ns	65	70
11	DIMM Configuration Type	Non-Parity		00	
12	Refresh Rate/Type	SR/1x(7.8us), Self Refresh Flag		82	
13	Primary DDR SDRAM Width	X8		08	
14	Error Checking DDR SDRAM Device Width	N/A		00	
15	DDR SDRAM Device Attr: Min Clk Delay, Random Col Access	1 Clock		01	
16	DDR SDRAM Device Attributes: Burst Length Supported	2,4,8		0E	
17	DDR SDRAM Device Attributes: Number of Device Banks	4		04	
18	DDR SDRAM Device Attributes: CAS Latencies Supported	2.5/3	2/25	18	0C
19	DDR SDRAM Device Attributes: CS Latency	0		01	
20	DDR SDRAM Device Attributes: WE Latency	1		02	
21	DDR SDRAM Device Attributes:	Differential Clock		20	
22	DDR SDRAM Device Attributes: General	+/-0.2V Voltage Tolerance		C0	
23	Minimum Clock Cycle at CL=2.5	6.0ns	7.5ns	60	75
24	Maximum Data Access Time (t_{AC}) from Clock at CL=2.5	0.7ns	0.75ns	70	75
25	Minimum Clock Cycle Time at CL=2	N/A		00	
26	Maximum Data Access Time (t_{AC}) from Clock at CL=2	N/A		00	
27	Minimum Row Precharge Time (t_{RP})	15ns	18ns	3C	48
28	Minimum Row Active to Row Active delay (t_{RRD})	10ns 12ns		28	30
29	Minimum RAS to CAS delay (t_{RCD})	15ns 18ns		3C	48
30	Minimum RAS Pulse Width (t_{RAS})	40ns	42ns	28	2A
31	Module Bank Density	512MB		80	
32	Address and Command Setup Time Before Clock	0.6ns	0.75ns	60	75
33	Address and Command Hold Time After Clock	0.6ns	0.75ns	60	75
34	Data Input Setup Time Before Clock	0.4ns	0.45ns	40	45
35	Data Input Hold Time After Clock	0.4ns	0.45ns	40	45
36-40	Reserved	Undefined		00	
41	Minimum Active/Auto-Refresh Time (tRC)	55ns	60ns	37	3C
42	SDRAM Device Minimum Auto-Refresh to Active/Auto Refresh Command Period (tRFC)	70ns	72ns	46	48
43	SDRAM Device Maximum Cycle Time (tCK max)	12		30	
44	SDRAM Device Maximum DQS-DQ Skew Time (tDQSQ)	0.4	0.45	28	2D
45	SDRAM Device Maximum Read Data Hold Skew Factor (tQHS)	0.5	0.55	50	55
46	Superset Information (may be used in future)	Undefined		00	
47	SDRAM device Attributes – DDR SDRAM DIMM Height	31.75mm		01	
48-61	Superset Information (may be used in future)	Undefined		00	
62	SPD Revision	1.0		10	
63	Checksum Data	Check sum		C7	57
64-71	Manufacturer's JEDED ID Code	0B Hex bank 3		7F7F7F0B00000000	
72-255	Reserved	Undefined		--	

SPD Values for 256MB

Byte	Description	SPD Entry Value		Serial PD Data Entry (Hexadecimal)	
		DDR400 -5T	DDR333 -6K	DDR400 -5T	DDR333 -6K
0	Number of Serial PD Bytes Written during Production	128		80	
1	Total Number of Bytes in Serial PD device	256		08	
2	Fundamental Memory Type	DDR SDRAM		07	
3	Number of Row Addresses on Assembly	13		0D	
4	Number of Column Addresses on Assembly	10		0A	
5	Number of DIMM Bank	1		01	
6.	Data Width of Assembly	X64		40	
7	Data Width of Assembly (cont')	X64		00	
8	Voltage Interface Level of this Assembly	SSTL 2.5V		04	
9	DDR SDRAM Device Cycle Time at CL=3	5ns	6ns	50	60
10	DDR SDRAM Device Access Time from Clock at CL=3	0.6ns	0.7ns	65	70
11	DIMM Configuration Type	Non-Parity		00	
12	Refresh Rate/Type	SR/1x(7.8us), Self Refresh Flag		82	
13	Primary DDR SDRAM Width	X16		10	
14	Error Checking DDR SDRAM Device Width	N/A		00	
15	DDR SDRAM Device Attr: Min Clk Delay, Random Col Access	1 Clock		01	
16	DDR SDRAM Device Attributes: Burst Length Supported	2,4,8		0E	
17	DDR SDRAM Device Attributes: Number of Device Banks	4		04	
18	DDR SDRAM Device Attributes: CAS Latencies Supported	2.5/3	2/2.5	18	0C
19	DDR SDRAM Device Attributes: CS Latency	0		01	
20	DDR SDRAM Device Attributes: WE Latency	1		02	
21	DDR SDRAM Device Attributes:	Differential Clock		20	
22	DDR SDRAM Device Attributes: General	+/-0.2V Voltage Tolerance		C0	
23	Minimum Clock Cycle at CL=2.5	6.0ns	7.5ns	60	75
24	Maximum Data Access Time (t_{AC}) from Clock at CL=2.5	0.7ns	0.75ns	70	75
25	Minimum Clock Cycle Time at CL=2	N/A		00	
26	Maximum Data Access Time (t_{AC}) from Clock at CL=2	N/A		00	
27	Minimum Row Precharge Time (t_{RP})	15ns	18ns	3C	48
28	Minimum Row Active to Row Active delay (t_{RRD})	10ns	12ns	28	30
29	Minimum RAS to CAS delay (t_{RCD})	15ns	18ns	3C	48
30	Minimum RAS Pulse Width (t_{RAS})	40ns	42ns	28	2A
31	Module Bank Density	256MB		40	
32	Address and Command Setup Time Before Clock	0.6ns	0.75ns	60	75
33	Address and Command Hold Time After Clock	0.6ns	0.75ns	60	75
34	Data Input Setup Time Before Clock	0.4ns	0.45ns	40	45
35	Data Input Hold Time After Clock	0.4ns	0.45ns	40	45
36-40	Reserved	Undefined		00	
41	Minimum Active/Auto-Refresh Time (tRC)	55ns	60ns	37	3C
42	SDRAM Device Minimum Auto-Refresh to Active/Auto Refresh Command Period (tRFC)	70ns	72ns	46	48
43	SDRAM Device Maximum Cycle Time (tCK max)	12		30	
44	SDRAM Device Maximum DQS-DQ Skew Time (tDQSQ)	0.4	0.45	28	2D
45	SDRAM Device Maximum Read Data Hold Skew Factor (tQHS)	0.5	0.55	50	55
46	Superset Information (may be used in future)	Undefined		00	
47	SDRAM device Attributes – DDR SDRAM DIMM Height	31.75mm		01	
48-61	Superset Information (may be used in future)	Undefined		00	
62	SPD Revision	Initial		10	
63	Checksum Data			8E	1E
64-71	Manufacturer's JEDED ID Code	0B Hex bank 3		7F7F7F0B00000000	
72-255	Reserved	Undefined		--	

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{IN}, V_{OUT}	Voltage on I/O pins relative to V_{SS}	-0.5 to V_{DDQ} +0.5	V
V_{IN}	Voltage on Input relative to V_{SS}	-0.5 to +3.6	V
V_{DD}	Voltage on V_{DD} supply relative to V_{SS}	-0.5 to +3.6	V
V_{DDQ}	Voltage on V_{DDQ} supply relative to V_{SS}	-0.5 to +3.6	V
T_A	Operating Temperature (Ambient)	0 to +70	℃
T_{STG}	Storage Temperature (Plastic)	-55 to +150	℃
P_D	Power Dissipation (per device component)	1	W
I_{OUT}	Short Circuit Output Current	50	mA

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics and Operating Conditions

T_A= 0℃ ~ 70℃; V_{DDQ}= V_{DD}= 2.5V±0.2V(6K); T_A= 0℃ ~ 70℃; V_{DDQ}= V_{DD}= 2.6V±0.1V(5T)

Symbol	Parameter		Min	Max	Units	Notes
V_{DD}	Supply Voltage	6K	2.3	2.7	V	1
		5T	2.5			
V_{DDQ}	I/O Supply Voltage	6K	2.3	2.7	V	1
		5T	2.5			
V_{SS}, V_{SSQ}	Supply Voltage, I/O Supply Voltage		0	0	V	
V_{REF}	I/O Reference Voltage		0.49 x V_{DDQ}	0.51 x V_{DDQ}	V	1, 2
V_{TT}	I/O Termination Voltage (System)		V_{REF} – 0.04	V_{REF} + 0.04	V	1, 3
$V_{IH\ (DC)}$	Input High (Logic1) Voltage		V_{REF} + 0.15	V_{DDQ} + 0.3	V	1
$V_{IL\ (DC)}$	Input Low (Logic0) Voltage		-0.3	V_{REF} - 0.15	V	1
$V_{IN\ (DC)}$	Input Voltage Level, CK and $\overline{CK}$ Inputs		-0.3	V_{DDQ} + 0.3	V	1
$V_{ID\ (DC)}$	Input Differential Voltage, CK and $\overline{CK}$ Inputs		0.30	V_{DDQ} + 0.6	V	1, 4
I_I	Input Leakage Current Any input 0V ≤ VIN ≤ V_{DD}; (All other pins not under test = 0V)		-10	10	µA	1
I_{OZ}	Output Leakage Current (DQs are disabled; 0V ≤ Vout ≤ V_{DDQ}		-10	10	µA	1
I_{OH}	Output High Current (V_{OUT} = V_{DDQ} -0.373V, min V_{REF}, min V_{TT})		-16.8	-	mA	1
I_{OL}	Output Low Current (V_{OUT} = 0.373, max V_{REF}, max V_{TT})		16.8	-	mA	1

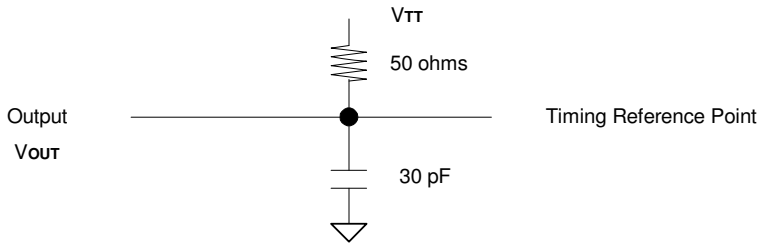
1. Inputs are not recognized as valid until V_{REF} stabilizes.
2. V_{REF} is expected to be equal to 0.5 V_{DDQ} of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed 2% of the DC value.
3. V_{TT} is not applied directly to the DIMM. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}.
4. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.

AC Characteristics

Notes 1-5 apply to the following Tables; Electrical Characteristics and DC Operating Conditions, AC Operating Conditions, Operating, Standby, and Refresh Currents, and Electrical Characteristics and AC Timing.)

1. All voltages referenced to V_{SS}.
2. Tests for AC timing, IDD, and electrical, AC and DC characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Outputs measured with equivalent load. Refer to the AC Output Load Circuit below.
4. AC timing and IDD tests may use a V_{IL} to V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK, $\overline{CK}$), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals is 1V/ns in the range between $V_{IL\,(AC)}$ and $V_{IH\,(AC)}$ unless otherwise specified.
5. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e. the receiver effectively switches as a result of the signal crossing the AC input level, and remains in that state as long as the signal does not ring back above (below) the DC input LOW (HIGH) level.

AC Output Load Circuits



AC Operating Conditions

Symbol	Parameter/Condition	Min	Max	Unit	Notes
$V_{IH\,(AC)}$	Input High (Logic 1) Voltage.	V_{REF} + 0.31		V	1, 2
$V_{IL\,(AC)}$	Input Low (Logic 0) Voltage.		V_{REF} - 0.31	V	1, 2
$V_{ID\,(AC)}$	Input Differential Voltage, CK and $\overline{CK}$ Inputs	0.62	V_{DDQ} + 0.6	V	1, 2, 3
$V_{IX\,(AC)}$	Input Differential Pair Cross Point Voltage, CK and $\overline{CK}$ Inputs	(0.5* V_{DDQ}) - 0.2	(0.5* V_{DDQ}) + 0.2	V	1, 2, 4

1. Input slew rate = 1V/ ns.
2. Inputs are not recognized as valid until V_{REF} stabilizes.
3. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
4. The value of V_{IX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the DC level of the same.

Operating, Standby, and Refresh Currents

T_A = 0 ℃ ~ 70 ℃; V_{DDQ}= V_{DD}= 2.5V ± 0.2V (6K); V_{DDQ}= V_{DD}= 2.6V ± 0.1V (5T)

Symbol	Parameter/Condition	Notes
IDD0	Operating Current: one bank; active/precharge; t_{RC} = $t_{RC\ (MIN)}$; t_{CK} = $t_{CK\ (MIN)}$; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	1,2
IDD1	Operating Current: one bank; active/read/precharge; Burst = 2; t_{RC} = $t_{RC\ (MIN)}$; CL=2.5; t_{CK} = $t_{CK\ (MIN)}$; I_{OUT} = 0mA; address and control inputs changing once per clock cycle	1,2
IDD2P	Precharge Power-Down Standby Current: all banks idle; power-down mode; CKE ≤ $V_{IL\ (MAX)}$; t_{CK} = $t_{CK\ (MIN)}$	1,2
IDD2N	Idle Standby Current: CS ≥ $V_{IH\ (MIN)}$; all banks idle; CKE ≥ $V_{IH\ (MIN)}$; t_{CK} = $t_{CK\ (MIN)}$; address and control inputs changing once per clock cycle	1,2
IDD3P	Active Power-Down Standby Current: one bank active; power-down mode; CKE ≤ $V_{IL\ (MAX)}$; t_{CK} = $t_{CK\ (MIN)}$	1,2
IDD3N	Active Standby Current: one bank; active/precharge; CS ≥ $V_{IH\ (MIN)}$; CKE ≥ $V_{IH\ (MIN)}$; t_{RC} = $t_{RAS\ (MAX)}$; t_{CK} = $t_{CK\ (MIN)}$; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	1,2
IDD4R	Operating Current: one bank; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; CL = 2.5; t_{CK} = $t_{CK\ (MIN)}$; I_{OUT} = 0mA	1,2
IDD4W	Operating Current: one bank; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; CL=2.5; t_{CK} = $t_{CK\ (MIN)}$	1,2
IDD5	Auto-Refresh Current: t_{RC} = $t_{RFC\ (MIN)}$	1,2,3
IDD6	Self-Refresh Current: CKE ≤ 0.2V	1,2
IDD7	Operating Current: four bank; four bank interleaving with BL = 4, address and control inputs randomly changing; 50% of data changing at every transfer; t_{RC} = $t_{RC\ (min)}$; I_{OUT} = 0mA.	1,2

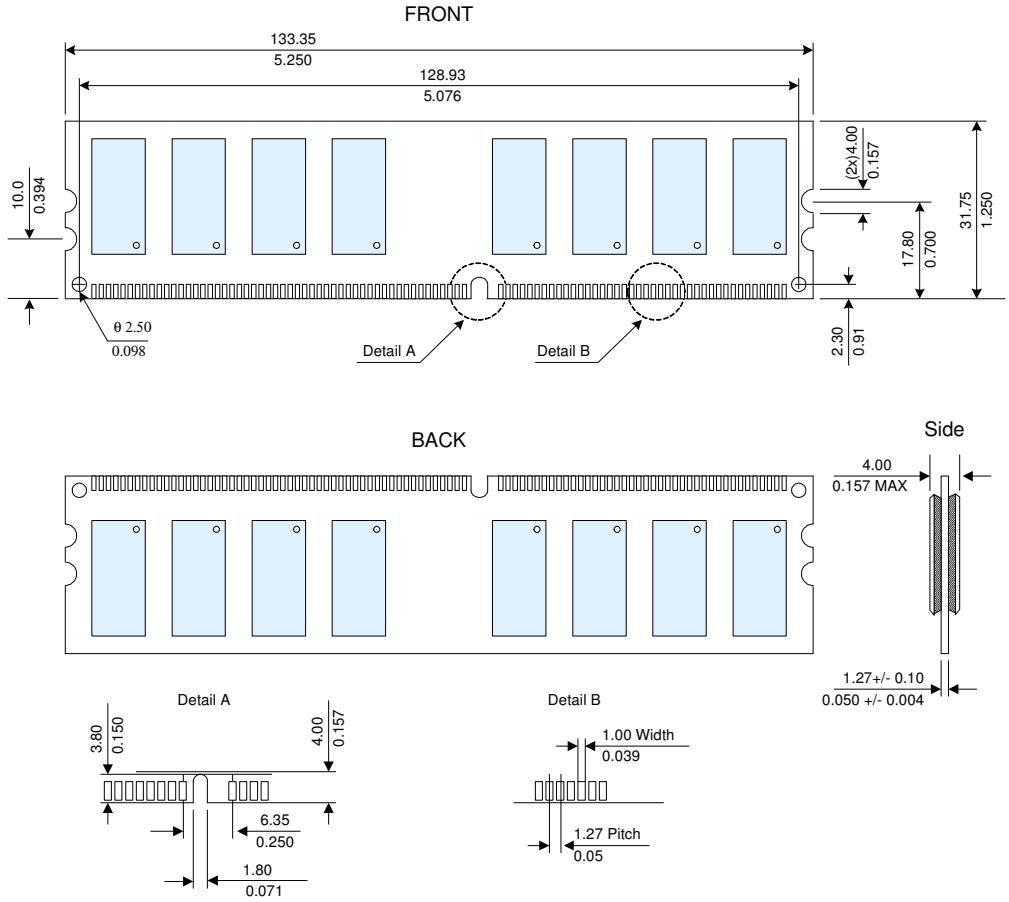
1. IDD specifications are tested after the device is properly initialized.
2. Input slew rate = 1V/ ns.
3. Current at 7.8 µs is time averaged value of IDD5 at $t_{RFC\ (MIN)}$ and IDD2P over 7.8 µs.

All IDD current values are calculated from device level.

	1GB		512MB		256MB		
Symbol (mA)	PC3200 (5T)	PC2700 (6K)	PC3200 (5T)	PC2700 (6K)	PC3200 (5T)	PC2700 (6K)	
IDD0	1651	1575	801	765	400	382	mA
IDD1	1702	1634	826	794	413	397	mA
IDD2P	60	57	28	27	14	13	mA
IDD2N	476	420	224	198	112	99	mA
IDD3P	211	195	99	92	50	46	mA
IDD3N	852	767	401	361	200	180	mA
IDD4R	2010	1705	980	830	490	415	mA
IDD4W	2195	1910	1072	932	536	466	mA
IDD5	3225	3125	1587	1540	794	770	mA
IDD6	37	38	17	18	9	9	mA
IDD7	5863	4961	2907	2458	1453	1229	mA

Package Dimensions

1GB, Non-ECC, 16 TSOP devices



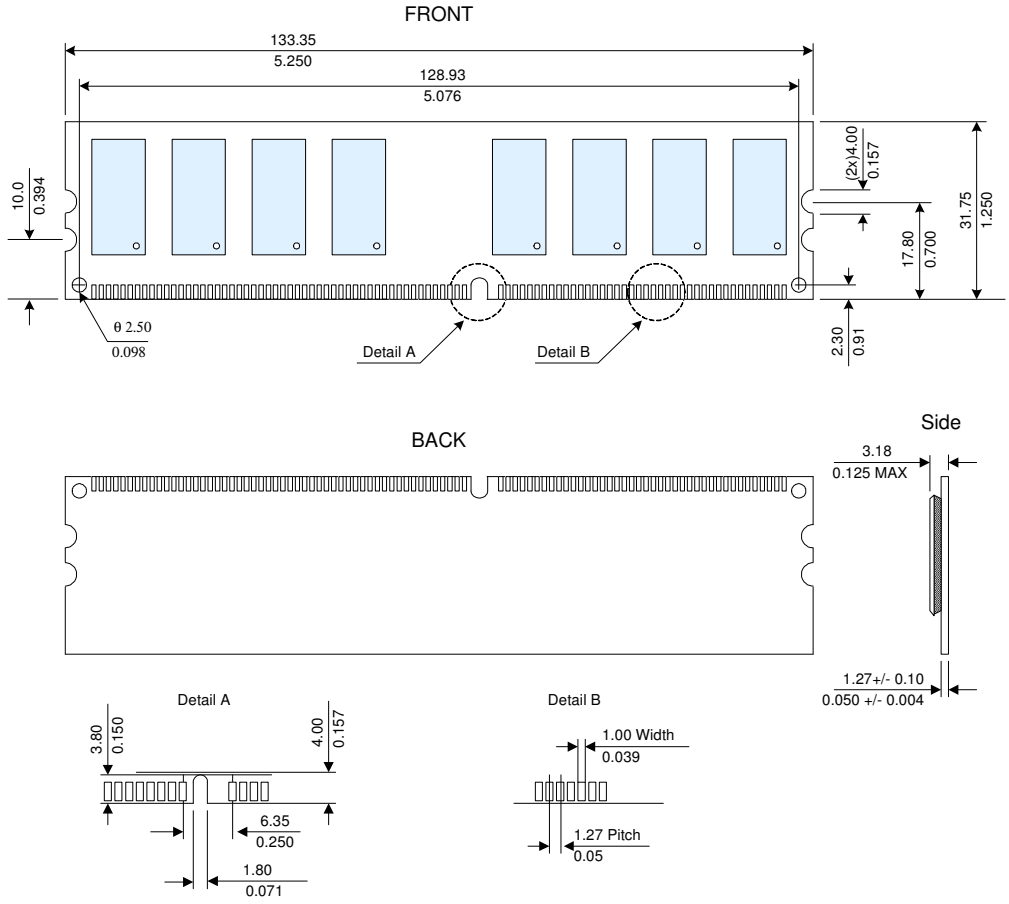
Note: All dimensions are typical with tolerances of +/- 0.15 (0.006) unless otherwise stated.

Units: Millimeters (Inches)

Note: Device packaging not drawn to scale. Placed only for references

Package Dimensions

512MB, Non-ECC, 8 TSOP devices



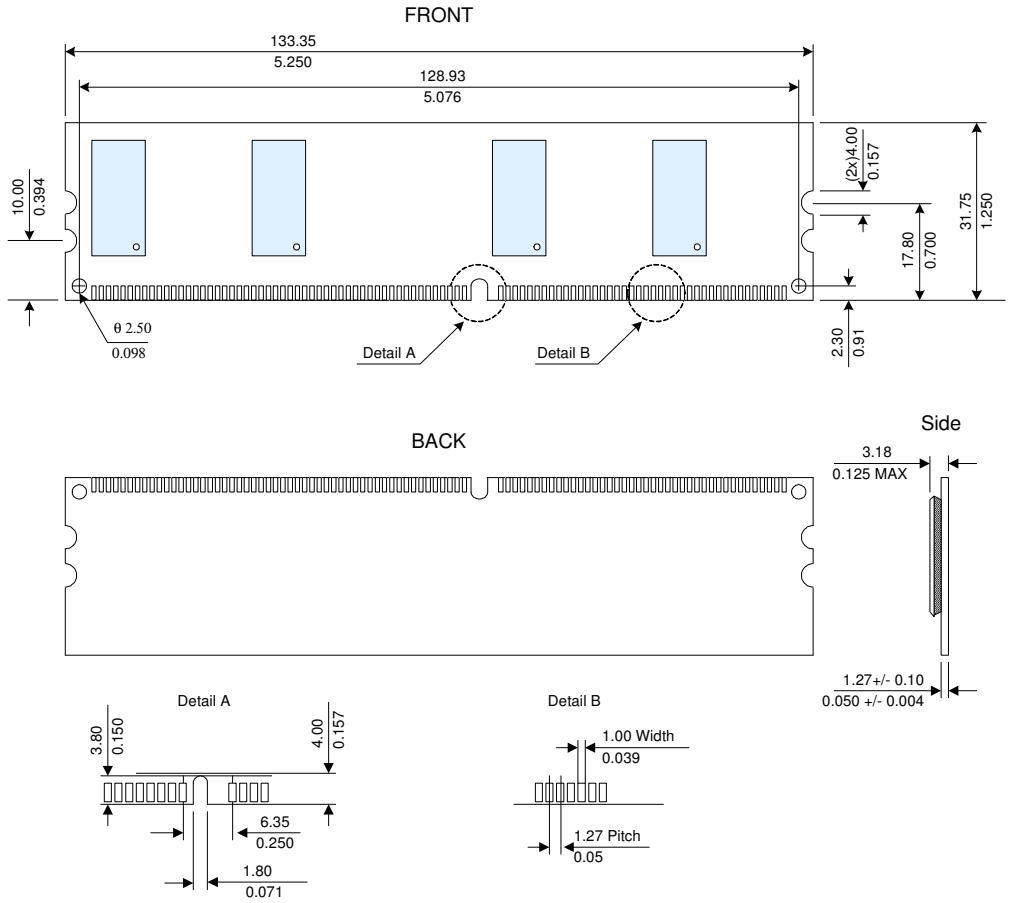
Note: All dimensions are typical with tolerances of +/- 0.15 (0.006) unless otherwise stated.

Units: Millimeters (Inches)

Note: Device packaging not drawn to scale. Placed only for references

Package Dimensions

256MB, Non-ECC, 4 TSOP devices



Note: All dimensions are typical with tolerances of +/- 0.15 (0.006) unless otherwise stated.

Units: Millimeters (Inches)

Note: Device packaging not drawn to scale. Placed only for references

Revision Log

Rev	Date	Modification
0.1	Jun 11,2004	Initial release: 1GB: M2U1G64DS8HB1G – 5T/6K, 512MB: M2U51264DS88B1G- 5T/6K 256MB: M2U25664DSH4B1G– 5T/6K
1.0	Nov 10, 2004	Updated: IDD333, IDD400, SPD for all modules
1.1	Nov 19, 2004	For Elixir module
1.2	June 2, 2006	Add Green products. M2Y1G64DS8HB1G – 5T/6K, M2Y51264DS88B1G- 5T/6K, M2Y25664DSH4B1G– 5T/6K